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**5** CASDAL 100%
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ACM Transactions on Database Systems (TODS) March 1978
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**7** Intel MMX for multimedia PCs 100%
Alex Peleg , Sam Wilkie , Uri Weiser
Communications of the ACM January 1997
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**8** Instruction issue logic for high-performance, interruptable pipelined processors 100%
G. S. Sohi , S. Vajapeyam
The 14th annual international symposium on Computer architecture June 1987

**9** The big three - today's 16-bit microprocessor 100%
R. K. Bell , W. D. Bell , T. C. Cooper , T. K. McFarland
Proceedings of the 13th micro-programming workshop on Microprogramming November 1980

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Ramon Canal , Antonio González , James E. Smith
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**12** Architecture of the IBM system/370 100%
Richard P. Case , Andris Padegs
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**13** A parallel bit map processor architecture for DA algorithms 100%
Tom Blank , Mark Stefik , Willem vanCleemput
Proceedings of the eighteenth design automation conference on Design automation June 1981

**14** Associative hardware and software techniques for integrity control 100%
Y. C. Hong , Stanley Y. W. Su
ACM Transactions on Database Systems (TODS) September 1981
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T. Okuma , H. Tomiyama , A. Inoue , E. Fajar , H. Yasuura
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Barry Shackleford , Mitsuhiro Yasuda , Etsuko Okushi , Hisao Koizumi , Hiroyuki Tomiyama , Hiroto Yasuura
Proceedings of the 34th annual conference on Design automation conference June 1997

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Supercomputing '88 November 1988

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J. Bradley Chen , Yasuhiro Endo , Kee Chan , David Mazières , Antonio Dias , Margo Seltzer , Michael D. Smith
ACM Transactions on Computer Systems (TOCS) February 1996
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**19** The measured performance of personal computer operating systems 100%
J. B. Chen , Y. Endo , K. Chan , D. Mazieres , A. Dias , M. Seltzer , M. D. Smith
ACM SIGOPS Operating Systems Review , Proceedings of the fifteenth ACM symposium on Operating systems principles December 1995
Volume 29 Issue 5

**20** Alpha AXP architecture 100%
Richard L. Sites
Communications of the ACM February 1993
Volume 36 Issue 2

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**1** 16-bit vs. 32-bit instructions for pipelined microprocessors 82%
John Bunda , Don Fussell , W. C. Athas , Roy Jenevein
ACM SIGARCH Computer Architecture News , Proceedings of the 20th annual international symposium on Computer architecture
May 1993
Volume 21 Issue 2

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**8** Dataflow machine architecture 100%
Arthur H. Veen
ACM Computing Surveys (CSUR) December 1986
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**9** I-NET mechanism for issuing multiple instructions 100%
L. Wang , C. L. Wu
Supercomputing '88 November 1988

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Jan-Willem Maessen , Xiaowei Shen
ACM SIGPLAN Notices , Proceedings of the conference on Object-oriented programming, systems, languages, and applications October 2000
Volume 35 Issue 10

**11** Code size minimization and retargetable assembly for custom EPIC and VLIW instruction formats 100%
Shail Aditya , Scott A. Mahlke , B. Ramakrishna Rau
ACM Transactions on Design Automation of Electronic Systems (TODAES) October 2000
Volume 5 Issue 4

**12** An environment for research in microprogramming and emulation 100%
Robert F. Rosin , Gideon Frieder , Richard H. Eckhouse
Communications of the ACM August 1972
Volume 15 Issue 8

**13** OHMEGA 100%
Masaitsu Nakajima , Hiraku Nakano , Yasuhiro Nakakura , Tadahiro Yoshida , Yoshiyuki Goi , Yuji Nakai , Reiji Segawa , Takeshi Kishida , Hiroshi Kadota
ACM SIGARCH Computer Architecture News , Proceedings of the 18th annual international symposium on Computer architecture April 1991
Volume 19 Issue 3

**14** Classifying load and store instructions for memory renaming 100%
Glenn Reinman , Brad Calder , Dean Tullsen , Gary Tyson , Todd Austin
Proceedings of the 1999 international conference on Supercomputing May 1999

**15** Tango 100%
Shlomit S. Pinter , Adi Yoaz
Proceedings of the 29th annual IEEE/ACM international

symposium on Microarchitecture December 1996

**16** Synthesis of instruction sets for pipelined microprocessors 100%
Ing-Jer Huang , Alvin M. Despain
Proceedings of the 31st annual conference on Design automation conference June 1994

**17** A case study in using two-level control stores 100%
Onat Menzilcioglu
Proceedings of the 20th annual workshop on Microprogramming December 1987

**18** An out-of-order superscalar processor with speculative execution and fast, precise interrupts 100%
Harry Dwyer , H. C. Torng
ACM SIGMICRO Newsletter , Proceedings of the 25th annual international symposium on Microarchitecture December 1992
Volume 23 Issue 1-2

**19** The architecture of the SPERRY UNIVAC 1100 series systems 100%
B. R. Borgerson , M. D. Godfrey , P. E. Hagerty , T. R. Rykken
Proceedings of the sixth annual symposium on Computer architecture April 1979

**20** Selective eager execution on the PolyPath architecture 100%
Artur Klauser , Abhijit Paithankar , Dirk Grunwald
ACM SIGARCH Computer Architecture News , Proceedings of the 25th annual international symposium on Computer architecture April 1998
Volume 26 Issue 3

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**1** A microprogrammed keyword transformation unit for a database computer 89%
Krishnamurthi Kannan , David K. Hsiao , Douglas S. Kerr
Proceedings of the tenth annual workshop on Microprogramming October 1977

The design of a microprogrammable microprocessor-based keyword transformation unit for a database computer(DBC) is described. The DBC, a specialized back-end computer capable of managing 109 - 1010 bytes of data, consists of two loops of memories and processors, the structure loop and the data loop, connected through a database command and control processor (DBCCP). The structure loop is used to retrieve and update the large amount (10

**2** The Clipper processor: instruction set architecture and implementation 87%
W. Hollingsworth , H. Sachs , A. J. Smith
Communications of the ACM February 1989
Volume 32 Issue 2

Intergraph's CLIPPER microprocessor is a high performance, three chip module that implements a new instruction set architecture designed for convenient programmability, broad functionality, and easy future expansion.

**3** Writing applications for uniform operation on a mainframe or PC: a metric conversion program 87%
Charles A. Schulz
ACM SIGAPL APL Quote Quad , Conference proceedings on APL 90: for the future May 1990
Volume 20 Issue 4

The metric system of measurement is the primary standard in all countries except the USA and two others. Use of the metric system is becoming more important to the USA for trade and commerce in the world economy. A metric conversion program was developed to convert 350 measurement units between inch-pound (or USA customary) and metric systems for engineering design and documentation. The program follows the primary national metric standard with its conversion factors and special rules for a ...

**4** The PL/EXUS language and virtual machine 85%
Gary A. Sitton , Thomas A. Kendrick , A. Gil Carrick
Proceedings of the ACM-IEEE symposium on High-level-language computer architecture November 1973

This paper describes a high level general purpose language which evolved from another high level systems programming language. As well, the compiler, pseudocode, and virtual machine are discussed in some detail. The new language is a powerful PL/1 dialect, as is its parent language, XPL 1. PL/EXUS (Programming Language/Extended XPL Users' S

**5** A history of the Promis technology: an effective human interface 85%

Jan Schultz
Proceedings of the ACM Conference on The history of personal workstations January 1986

Scientific computing systems for individuals were pioneered early at Hewlett-Packard, beginning with the 9100A Desktop Calculator in 1968. Extensions of this first machine were soon seen in Personal Peripherals, such as Printers, Tape Cartridges, and Plotters, and followed by Graphic CRT Displays. By early 1972, the Desktop unit had been augmented by a very powerful Pocket Calculator, the ground-breaking HP 35A.This paper traces the evolution of these machines to the present day, ...

**6** A Cost Model for the Internal Organization of B+-Tree Nodes 84%
Wilfred J. Hansen
ACM Transactions on Programming Languages and Systems (TOPLAS) October 1981
Volume 3 Issue 4

**7** Information Content of Programs and Operation Encoding 84%
Eric C. R. Hehner
Journal of the ACM (JACM) April 1977
Volume 24 Issue 2

The problem of determining the minimum representation of programs for execution by a computer is considered. The methods of measuring space requirements suggest practical methods for encoding programs and for designing machine languages. An analysis of the operation portion of instructions finds that the 47 operation codes used by a well-known compiler require, on average, fewer than two bits each.

**8** Variable length path branch prediction 84%
Jared Stark , Marius Evers , Yale N. Patt
Proceedings of the 8th international conference on Architectural support for programming languages and operating systems October 1998

**9** Improving code density using compression techniques 84%

Charles Lefurgy , Peter Bird , I-Cheng Chen , Trevor Mudge
Proceedings of the thirtieth annual IEEE/ACM international symposium on Microarchitecture December 1997

**10** A model for dataflow based vector execution 84%
W. Marcus Miller , Walid A. Najjar , A. P. Wim Böhm
Proceedings of the 8th conference on ACM international conference on supercomputing July 1994

Although the dataflow model has been shown to allow the exploitation of parallelism at all levels, research of the past decade has revealed several fundamental problems: Synchronization at the instruction level, token matching, coloring and re-labeling operations have a negative impact on performance by significantly increasing the number of non-compute “overhead” cycles. Recently, many novel Hybrid von-Neumann Data Driven machines have been proposed to alleviate some of these p ...

**11** Hardware speedups in long integer multiplication 82%
M. Shand , P. Bertin , J. Vuillemin
Proceedings of the second annual ACM symposium on Parallel algorithms and architectures May 1990

**12** An approach to standardizing computer systems 82%
Edward Morenoff , John B. McLean
Proceedings of the twenty second national conference January 1967

The fundamental goal of an evolutionary approach to upgrading a computer installation is the maintenance of a continuity of operation as various elements of the installation (equipment components and system support programs) are replaced. The realization of this goal requires the isolation and separation of the inter-dependencies which now exist between the various elements of a computer installation. This includes the inter-dependencies between programs and the characteristics of equipment ...

**13** A microprogram simulator 82%
Steve Young
Proceedings of the June 1971 design automation workshop on

Design automation June 1971

Micro-programming has been defined as an orderly approach to the design of a control section of a computer using control signals arranged in fixed-length words. The control section is the part of a computer which controls the activities of the memories, the central processing unit, the arithmetic unit and the peripheral units. The most elementary operation is called a micro-operation. Such an operation could be a comparison of two registers or a register to register t ...

**14** A Self Managing Secondary Memory system 82%

Manlio DeMartinis , G. Jack Lipovski , Stanley Y.W. Su , J. K. Watson

Proceedings of the third annual symposium on Computer architecture January 1976

A Self Managing Secondary Memory (SMSM) organization is proposed herein, in which hardware directly assists the storage, retrieval and management of arbitrary length records on such devices as fixed head discs or charge coupled devices (CCD's). This paper emphasizes some of the techniques used to implement an SMSM system. In an SMSM, fixed length words are organized into variable length records, and these records are packed into a file. The first word of the record, a label, can ...

**15** Run-time checking in Lisp by integrating memory addressing and range checking 82%

M. Sato , S. Ichikawa , E. Goto

ACM SIGARCH Computer Architecture News , Proceedings of the 16th annual international symposium on Computer architecture April 1989

Volume 17 Issue 3

This paper describes the BL addressing mode and the address tag in FLATS2 machine, which is a general-purpose MIMD computer now under construction. The BL addressing mode integrates memory accessing and range checking by hardware. Address tag is a bit in word, which indicates the capability for memory access. Combining them together, efficient memory protection is provided at run-time. It reduces the cost of run-time type checking in Lisp by

checking the address tag and the address of a poi ...

**16** A unified vector/scalar floating-point architecture 82%
N. P. Jouppi , J. Bertoni , D. W. Wall
ACM SIGARCH Computer Architecture News , Proceedings of the third international conference on Architectural support for programming languages and operating systems April 1989
Volume 17 Issue 2

In this paper we present a unified approach to vector and scalar computation, using a single register file for both scalar operands and vector elements. The goal of this architecture is to yield improved scalar performance while broadening the range of vectorizable applications. For example, reduction operations and recurrences can be expressed in vector form in this architecture. This approach results in greater overall performance for most applications than does the approach of emphasizin ...

**17** RUNCIBLE—algebraic translation on a limited computer 82%
Donald E. Knuth
Communications of the ACM November 1959
Volume 2 Issue 11

**18** Implications of structured programming for machine architecture 82%
Andrew S. Tanenbaum
Communications of the ACM March 1978
Volume 21 Issue 3

Based on an empirical study of more than 10,000 lines of program text written in a GOTO-less language, a machine architecture specifically designed for structured programs is proposed. Since assignment, CALL, RETURN, and IF statements together account for 93 percent of all executable statements, special care is given to ensure that these statements can be implemented efficiently. A highly compact instruction encoding scheme is presented, which can reduce program size by a factor of 3. Unlik ...

**19** Algorithm 607: Text Exchange System: A Transportable 82%

System for Management and Exchange of Programs and other Text
W. V. Snyder , R. J. Hanson
ACM Transactions on Mathematical Software (TOMS) December 1983
Volume 9 Issue 4

**20** The hardware architecture of the CRISP microprocessor 82%
D. R. Ditzel , H. R. McLellan , A. D. Berenbaum
The 14th annual international symposium on Computer architecture June 1987

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**1** Performance evaluation of a decoded instruction cache for variable instruction-length computers 82%
Gideon Intrater , Ilan Spillinger
ACM SIGARCH Computer Architecture News , Proceedings of the 19th annual international symposium on Computer architecture
April 1992
Volume 20 Issue 2

A Decoded INstruction Cache (DINC) serves as a buffer between the instruction decoder and the other instruction-pipeline stages. In this paper we explain how techniques that reduce the branch penalty based on such a cache, can improve CPU performance. We analyze the impact of some of the design parameters of DINCs on variable instruction-length computers, e.g., CISC machines. Our study indicates that tuning the mapping function of the instructions into the cache, can improve the ...

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1 **Bit permutation instructions for accelerating software cryptograph**
*Zhijie Shi; Lee, R.B.*
Application-Specific Systems, Architectures, and Processors, 2000. Proceedi
International Conference on , 2000
Page(s): 138 -148

[Abstract] [PDF Full-Text (220 KB)] **CNF**

2 **The SH microprocessor: 16-bit fixed length instruction set provide power and die size**
*Freet, P.*
Compcon Spring '94, Digest of Papers. , 1994
Page(s): 486 -488

[Abstract] [PDF Full-Text (196 KB)] **CNF**

3 **A unique instructional tool for visualizing equipotentials and its us introductory fields course**
*Lyvers, R.F.; Horowitz, B.R.*
Education, IEEE Transactions on , Volume: 36 Issue: 2 , May 1993
Page(s): 237 -240

[Abstract] [PDF Full-Text (352 KB)] **JNL**

4 **16-bit Vs. 32-bit Instructions For Pipelined Microprocessors**
*Bunda, J.; Fussell, D.; Athas, W.C.; Jenevein, R.*
Computer Architecture, 1993., Proceedings of the 20th Annual International

Symposium on , 1993
Page(s): 237 -246

[Abstract] [PDF Full-Text (704 KB)] **CNF**

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5 **Applications of a Courseware For Cai of Electromagnetic Field Thec Instruction**
*Wang Rui-yu; Qian Xiu-ying; Wang Fang*
Electromagnetic Field Computation, 1992. Digest of the Fifth Biennial IEEE C on
Page(s): WP21 -WP21

[Abstract] [PDF Full-Text (92 KB)] **CNF**

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6 **A 64-bit floating-point processing unit with a horizontal instructioı parallel operations**
*Katsuno, A.; Takahashi, H.; Kubosawa, H.; Sato, T.; Suga, A.; Goto, G.*
Computer Design: VLSI in Computers and Processors, 1990. ICCD '90. Proce 1990 IEEE International Conference on , 1990
Page(s): 347 -350

[Abstract] [PDF Full-Text (312 KB)] **CNF**

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7 **Computer aided electromagnetic field instruction on Project Athen**
*Kirtley, J.L., Jr.*
Antennas and Propagation Society International Symposium, 1990. AP-S. M Technologies for the 90's. Digest. , 1990
Page(s): 1685 -1688 vol.4

[Abstract] [PDF Full-Text (148 KB)] **CNF**

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8 **A 32-bit microprocessor with high performance bit-map manipulat instructions**
*Shimizu, T.; Iwata, S.; Saito, Y.; Yoshida, T.; Matsuo, M.; Hinata, J.; Saito,*
Computer Design: VLSI in Computers and Processors, 1989. ICCD '89. Proce 1989 IEEE International Conference on , 1989
Page(s): 406 -409

[Abstract] [PDF Full-Text (256 KB)] **CNF**

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1 **High-performance extendable instruction set computing**
*Heui Lee; Beckett, P.; Appelbe, B.*
Computer Systems Architecture Conference, 2001. ACSAC 2001. Proceeding
Australasian , 2001
Page(s): 89 -94

[Abstract] [PDF Full-Text (500 KB)] **CNF**

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2 **Application domains for fixed-length block structured architecture**
*Eeckhout, L.; Vander Aa, T.; Goeman, B.; Vandierendonck, H.; Lauwereins, Bosschere, K.*
Computer Systems Architecture Conference, 2001. ACSAC 2001. Proceeding
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3 **An integrated circuit/architecture approach to reducing leakage in deep-submicron high-performance I-caches**
*Yang, S.; Powell, M.D.; Falsafi, B.; Roy, K.; Vijaykumar, T.N.*
High-Performance Computer Architecture, 2001. HPCA. The Seventh Interna
Symposium on , 2001
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[Abstract] [PDF Full-Text (1096 KB)] **CNF**

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4 **Reducing leakage in a high-performance deep-submicron instructi**
*Powell, M.; Se-Hyun Yang; Falsafi, B.; Roy, K.; Vijaykumar, N.*

Very Large Scale Integration (VLSI) Systems, IEEE Transactions on , Volum
1 , Feb. 2001
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[Abstract] [PDF Full-Text (228 KB)] **JNL**

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5 **SimpleFit: a framework for analyzing design trade-offs in Raw arcl**

*Moritz, C.A.; Donald Yeung; Agarwal, A.*
Parallel and Distributed Systems, IEEE Transactions on , Volume: 12 Issue:
2001
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6 **An embedded 16-bit microprocessor**
*Young-Ho Cha; Chang-Su Park; Gyeong-Yeon Cho; Hyek-Hwan Choi*
ASICs, 2000. AP-ASIC 2000. Proceedings of the Second IEEE Asia Pacific Co
on , 2000
Page(s): 335 -338

[Abstract] [PDF Full-Text (280 KB)] **CNF**

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7 **An area efficient video/audio codec for portable multimedia applic**
*Seongmo Park; Seongmin Kim; Kyeongjin Byeon; Jinjong Cha; Hanjin Cho*
Circuits and Systems, 2000. Proceedings. ISCAS 2000 Geneva. The 2000 IE
International Symposium on , Volume: 1 , 2000
Page(s): 595 -598 vol.1

[Abstract] [PDF Full-Text (392 KB)] **CNF**

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8 **On the feasibility of fixed-length block structured architectures**
*Eeckhout, L.; De Bosschere, K.; Neefs, H.*
Computer Architecture Conference, 2000. ACAC 2000. 5th Australasian , 19
Page(s): 17 -25

[Abstract] [PDF Full-Text (188 KB)] **CNF**

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9 **High-performance DSPs**
*Junchen Du; Warner, G.; Vallow, E.; Hollenbach, T.*
IEEE Signal Processing Magazine , Volume: 17 Issue: 2 , March 2000

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[Abstract] [PDF Full-Text (368 KB)] **JNL**

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10 **Probabilistic loop scheduling for applications with uncertain exec time**
*Tongsima, S.; Sha, E.H.-M.; Chantrapornchai, C.; Surma, D.R.; Passos, N.L.*
Computers, IEEE Transactions on , Volume: 49 Issue: 1 , Jan. 2000
Page(s): 65 -80

[Abstract] [PDF Full-Text (592 KB)] **JNL**

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11 **Implementation of 13 kbps QCELP vocoder ASIC**
*Kyung-Jin Byun; Minsoo Hahn; Kyung-Su Kim*
ASICs, 1999. AP-ASIC '99. The First IEEE Asia Pacific Conference on , 1999
Page(s): 258 -261

[Abstract] [PDF Full-Text (340 KB)] **CNF**

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12 **Exploring instruction-fetch bandwidth requirement in wide-issue superscalar processors**
*Michaud, P.; Seznec, A.; Jourdan, S.*
Parallel Architectures and Compilation Techniques, 1999. Proceedings. 1999 International Conference on , 1999
Page(s): 2 -10

[Abstract] [PDF Full-Text (148 KB)] **CNF**

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13 **Design of a combined processor containing a 32-bit RISC micropr and a 16-bit fixed-point DSP on a chip**
*Wookyeong Jeong; Sangjun An; Moongyung Kim; Sangkyong Heo; Youngjui Sangook Moon; Yongsurk Lee*
VLSI and CAD, 1999. ICVC '99. 6th International Conference on , 1999
Page(s): 305 -308

[Abstract] [PDF Full-Text (332 KB)] **CNF**

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14 **Generation of interpretive and compiled instruction set simulator:**
*Leupers, R.; Elste, J.; Landwehr, B.*
Design Automation Conference, 1999. Proceedings of the ASP-DAC '99. Asia Pacific , 1999

Page(s): 339 -342 vol.1

[Abstract] [PDF Full-Text (372 KB)] **CNF**

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15 **Investigating the implementation of a block structured processor architecture in an early design stage**
*Eeckhout, L.; Neefs, H.; De Bosschere, K.; Van Campenhout, J.*
EUROMICRO Conference, 1999. Proceedings. 25th , Volume: 1 , 1999
Page(s): 186 -193 vol.1

[Abstract] [PDF Full-Text (744 KB)] **CNF**

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16 **PipeRench: a coprocessor for streaming multimedia acceleration**
*Goldstein, S.C.; Schmit, H.; Moe, M.; Budiu, M.; Cadambi, S.; Taylor, R.R.;*
Computer Architecture, 1999. Proceedings of the 26th International Sympos
1999
Page(s): 28 -39

[Abstract] [PDF Full-Text (164 KB)] **CNF**

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17 **A real-time digital VCR encode/decode and MPEG-2 decode LSI implemented on a dual-issue RISC processor**
*Mohri, A.; Yamada, A.; Yoshida, Y.; Sato, H.; Takata, H.; Nakakimura, K.; H M.; Shimotsuma, Y.; Tsuchihashi, K.*
Solid-State Circuits, IEEE Journal of , Volume: 34 Issue: 7 , July 1999
Page(s): 992 -1000

[Abstract] [PDF Full-Text (328 KB)] **JNL**

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18 **Synthesis of application specific instructions for embedded DSP s**
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| 1 | 39 | (register adj file) near3 (simultaneous near3 (access or read or write)) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB | 2001/12/19 17:55 |
| 8 | 1666 | "SIMD" | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB | 2001/12/19 16:41 |
| 22 | 50 | (bit near3 locations)same (instruction adj format) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB | 2001/12/19 16:47 |
| 15 | 7 | "SIMD" and (simultaneous$2 near3 execut$3 near3 (single or one) near3 instruction) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB | 2001/12/19 16:44 |
| 29 | 6 | (bit near3 locations) with (instruction adj format) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB | 2001/12/19 16:48 |
| 36 | 1022198 | WO 92/08230.pn. | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB | 2001/12/19 17:56 |
| 43 | 0 | WO92/08230.pn. | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB | 2001/12/19 17:56 |
| - | 31771 | instruction near3 set | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB | 2001/12/19 07:45 |
| - | 400 | (instruction near3 set) same (fixed near3 (length or size or bit$2)) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB | 2001/12/17 12:24 |
| - | 307 | (instruction near3 set) same (fixed adj (length or size or bit$2)) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB | 2001/12/17 12:25 |
| - | 201 | (instruction near3 set) with (fixed adj (length or size or bit$2)) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB | 2001/12/17 12:30 |
| - | 84 | ((instruction near3 set) with (fixed adj (length or size or bit$2))) with (tag$2 or bit$2 or flag$2) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB | 2001/12/17 12:30 |

| | | | | |
|---|---|---|---|---|
| - | 51 | ((instruction near3 set) with (fixed adj (length or size or bit$2))) same ((dual or two or multiple or plural) near3 (operations or instructions)) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB | 2001/12/17 15:37 |
| - | 394225 | compound.ti. | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB | 2001/12/17 14:02 |
| - | 41 | compound.ti. and instruction.ti. | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB | 2001/12/17 14:26 |
| - | 1 | EP-992892-$.DID. | DERWENT | 2001/12/17 14:06 |
| - | 10 | krishnan.in. and "hitachi ltd".as. | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB | 2001/12/17 14:37 |
| - | 120 | 712/24.ccls. | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB | 2001/12/17 14:38 |
| - | 7 | catan.in. and texas$.as. | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB | 2001/12/17 14:41 |
| - | 324 | 712/215.ccls. | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB | 2001/12/18 10:07 |
| - | 2399 | (packed or compound or combined or grouped) near3 instruction$2 | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB | 2001/12/18 10:08 |
| - | 175 | ((dual or two) near2 operation$2) with ((single or one) near2 instruction) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB | 2001/12/18 10:10 |
| - | 19253 | "texas instruments".as. | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB | 2001/12/18 10:10 |
| - | 0 | "texas instruments".as. and (compound near3 instruction$2) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB | 2001/12/18 10:49 |
| - | 25 | ((packed or compound or combined or grouped) near3 instruction$2) same (fixed near3 (length or size or bits)) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB | 2001/12/18 10:37 |

| | | | | |
|---|---|---|---|---|
| - | 44 | (((dual or two) near2 operation$2) with ((single or one) near2 instruction)) same (field or flag or bit or tag) | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB | 2001/12/18 10:40 |
| - | 2 | ("6115806").PN. | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB | 2001/12/18 14:09 |
| - | 2 | ("6292845").PN. | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB | 2001/12/19 07:45 |
| - | 0 | 6292845.URPN. | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB | 2001/12/19 07:46 |
| - | 50 | ("4114026" \| "4236206" \| "4280177" \| "4502111" \| "4530050" \| "4654781" \| "4888679" \| "5051885" \| "5201056" \| "5371864" \| "5488710" \| "5537629" \| "5898851" \| "5938759" \| "5987235" \| "6012137" \| "6134650" \| "6170050").PN. | USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM TDB | 2001/12/19 07:54 |
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